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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,669	10/30/2001	Youfeng Wu	42390P10350	7939

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
NGUYEN BA, HOANG VU A	
ART UNIT	**PAPER NUMBER**
2122	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,669	WU ET AL.	
	Examiner	Art Unit	
	Hoang-Vu A Nguyen-Ba	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/12/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed October 30, 2001.

2. The priority date considered for this application is October 30, 2001.

3. Claims 1-19 have been examined.

Drawings

4. The drawings filed October 30, 2001 are objected to because of the following minor informalities:

a. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

b. Figure 2: The instruction "ASSERT a==2" in block 235 should be labeled with reference number – 260 --.

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The abstract of the disclosure is objected to because of the following minor informality: the preposition "of" at the end of line 8 should be deleted.

Correction is required. See MPEP § 608.01(b).

Claim Objection

6. Claims 1, 8 and 14 are objected to because of the following informalities:

a. Claims 1 (line 8) and 8 (line 7): a conjunction – and – should be added at the end of the limitation that precedes the last limitation of the claim;

b. Claim 14: the preposition "of" after "results" in line 7 should be deleted.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1, 7, 8, 13, 14 and 19 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claims 1, 8 and 14 recite the limitation "*using compiler transformation and hardware support to handle infrequently executed code.*" This limitation is found to be vague, unclear and thus indefinite because it is not clear whether this limitation is to be interpreted as being:

i. a compilation technique that uses well-known techniques of promoting branch and forming regions or **frames** (see rePLay by Patel and Lumetta), which are large single-entry, single-exit regions spanning many blocks in a program's dynamic instruction stream, wherein infrequent executed code is removed (i.e., *to handle infrequently executed code* by eliminating the code from the region); or

ii. a compilation technique of how to specifically handle the infrequently executed code after the infrequently executed code has been eliminated from the regions formed by the rePLay technique.

For art rejection purposes, the above limitation is interpreted as being discussed in i.

b. Claims 7, 13 and 19 recite the limitation "*the compiler improves performance of the computer program by updating a branch frequency for an original code corresponding to the region to form an improved region*," which is found to be vague and indefinite. First, it is unclear how performance of a computer program can be improved by updating a branch frequency. Second, it is not clear which frequency is being referred to? Is it the number of times a branch has had the same outcome consecutively? Third, it is not clearly understood what *an original code corresponding to the region* is. Last, it is not clear what *an improved region* is.

For art rejection purposes, the limitation recited in claims 7, 13 and 19 is interpreted to mean that the compiler improves performance of the computer program by promoting and converting a branch into an ASSERT instruction in a frame if the number of times a branch has had the same outcome consecutively reaches a threshold. See rePLay, third paragraph of section 4.

Claim Rejections - 35 U.S.C. § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-19 are rejected under 35 U.S.C. § 102(b) as being anticipated by Patel-Lumetta's "rePLay: a Hardware Framework for Dynamic Program Optimization," December 1999 ("rePLay").

Claim 1

rePLay discloses at least:

a compiler to compile a computer program, the compiler forming optimized code regions to improve performance of the computer program by optimizing frequently executed code and using compiler transformation and hardware support to handle infrequently executed code (see at least section 2 – The rePLay Framework –; for *forming optimized code regions*, see "Frame Construction" discussion; for *using compiler transformation and hardware support to handle infrequently executed code*, see "ASSERT firing," "Sequencing Model" discussions throughout the article);

a memory to store the compiler (see at least page 2, line 2, "... a flexible optimizer contained within the processor."; section 2.1, e.g., "... a piece of an optimizing compiler is embedded within the processor hardware");

a central processing unit (CPU) cooperatively connected to the memory to run the compiler and to speculatively execute the optimized code regions (see at least Figure 1, e.g., "Execution Engine" and related discussion in the article); and

a store buffer connected to the CPU to improve the speed at which the CPU speculatively executes the optimized code regions (see at least Figure 1, e.g., "Frame cache" and related discussion in the article).

Claim 8

rePLay discloses at least:

compiling a computer program (see at least section 2, "The rePLay framework which uses information on highly biases branch gathered from profile executions of a program to optimize an application's instruction stream);

improving performance of the computer program by optimizing frequently executed code and using compiler transformation and hardware support to handle infrequently executed code (see at least section 5, "Sequencing Model");

storing temporarily the results produced during execution of formed regions to handle infrequent code being actually executed (see at least Figure 11, e.g., "Conventional Branch Pred w/ BTB" and related discussion in the article); and

committing the results produced when the execution of the region is completed sucessfully (see at least section 4, "Frame Construction"; see discussion on Branch Promotion and ASSERT instructions).

Claim 14

Claim 14 recites a machine-readable medium comprising instructions which, when executed by a machine cause the machine to perform the same method steps of claim 8. As a result, claim 14 is rejected under 35 U.S.C. § 102(b) as being anticipated by rePLay for the same reasons.

Claim 2

The rejection of base claim 1 is incorporated. rePLay further discloses *wherein the store buffer assists the CPU in speculatively executing the optimized code regions by temporarily storing results produced during the speculative execution of the optimized code regions* (see at least Figure 1, e.g., "Frame cache" and related discussion in the article).

Claims 3, 9 and 15

Rejections of base claims 1, 8 and 14 respectively are incorporated. rePLay further discloses *wherein the compiler improves performance of the computer program by applying standard available optimizations* (see at least section 2.4, e.g., "...The range of optimization includes classical optimizations...").

Claims 4, 10 and 16

Rejections of base claims 1, 8 and 14 respectively are incorporated. rePLay further discloses *wherein the compiler improves performance of the computer program by selecting a seed block, duplicating the seed block, and growing the seed block to form a region* (see at least Figure 3 and related discussion in the article; seed block A is selected, duplicated in frame ABCDE and grown to form frame ABCDE).

Claims 7, 13 and 19

Rejections of base claims 1, 8, 14 and intervening claims 4, 10, 16 respectively are incorporated. rePLay further discloses *wherein the compiler improves performance of the computer program by updating a branch frequency for an original code corresponding to the region to form an improved region* (see at least section 4, "Frame Construction").

Claim Rejections - 35 USC § 103

11. The following is a quotation of the 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in

the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 5, 6, 11, 12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over rePLay, as applied to the base and intervening claims, in view of Patel-Evers-Patt, Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing ("Patel").

Claims 5, 11 and 17

Rejections of base claims 1, 8, 14 and intervening claims 4, 10, 16 respectively are incorporated. rePLay does not specifically disclose *wherein the compiler improves performance of the computer program by trimming blocks near a head block of the region to form a trimmed region having improved scheduling cycles*. However, Patel teaches a trace packing technique which consists of packing trace segments with as many as instructions as will fit in order to improve the number of instructions delivered each cycle by the trace cache. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Patel to pack rePLay's frame with as many branch instructions that are frequently executed as will fit because this would trim the rePLay's frame's head and tail out of branch instructions that cannot be promoted, thereby improving the process of obtaining a better frame for further aggressive optimization.

Claims 6, 12 and 18

Rejections of base claims 1, 8, 14 and intervening claims 4, 10, 16 respectively are incorporated. rePLay does not specifically disclose *wherein the compiler improves performance of the computer program by trimming blocks near a tail block of the region to form a trimmed region having improved scheduling cycles*. However, Patel teaches a trace packing

technique which consists of packing trace segments with as many as instructions as will fit in order to improve the number of instructions delivered each cycle by the trace cache. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Patel to pack rePLay's frame with as many branch instructions that are frequently executed as will fit because this would trim the rePLay's frame's head and tail out of branch instructions that cannot be promoted, thereby improving the process of obtaining a better frame for further aggressive optimization.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Vu A Nguyen-Ba whose telephone number is (703) 305-0103. The examiner can normally be reached on Tuesday-Friday, 6:00 – 16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Dam can be reached on (703) 305-4552. After October 25, 2004, the examiner can be reached at (571) 272-3701 and the examiner's supervisor at (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANTONY NGUYEN-BA
PRIMARY EXAMINER

Art Unit 2122

September 03, 2004